CLAIMS

1. A context based direct memory access architecture, comprising:

a memory;

a plurality of ports, wherein each port has an associated buffer for temporarily storing data transferred through the port, and wherein each port has an associated direct memory access channel;

a direct memory access controller that receives requests for accessing the memory by the plurality of ports, wherein each request is received from one of the plurality of ports, and wherein the direct memory access controller stores parameters defining the direct memory access operations for each port, and wherein after a request is received from a port the direct memory access controller loads the parameters for the current direct memory access operation for the port to enable the port to access the memory.

2. The context based DMA of claim 1, further comprising a central parameter store for storing parameters for each of a plurality of DMA channels corresponding to each of the plurality of ports.

3. The context based DMA of claim 2, wherein the direct memory access controller further comprises means for servicing the request, comprising:

means for queuing a memory operation;

means for updating parameters; and

means for fetching and storing parameters in the central parameter store.

4. An apparatus for communicating data among devices interconnected by a memory, comprising;

a single DMA controller;

in the first device, means for writing data to the memory using the DMA controller;

in the second device, means for reading data from the memory using the DMA controller;

wherein the DMA controller receives information from a DMA context memory specifying parameters for writing data from the first device to the memory and wherein the DMA controller receives information from the DMA context memory specifying parameters for reading data from the memory to the second device.

5. The apparatus of claim 4, further comprising:

a buffer control unit for communicating to the DMA controller an indication of an amount of data written into the memory by the first device through the DMA controller and for communicating to the DMA controller an indication of the amount of data read from the memory by the second device through the DMA controller; and

wherein the DMA controller reads data from the memory for the second device if data is available as determined by the indicated amount of data written to the memory and the amount of data read from the memory as communicated by the buffer control unit.

6. The apparatus of claim 4, further comprising:

a buffer control unit for communicating to the DMA controller an indication of an amount of data written into the memory by the first device through the DMA controller and for communicating to the DMA controller an indication of the amount of data read from the memory by the second device through the DMA controller; and

wherein the DMA controller writes data to the memory for the first device if memory space is available as determined by the indicated amount of data written to the memory and the amount of data read from the memory as communicated by the buffer control unit.